

WHAT IS CLAIMED IS:

1. An antifuse comprising:
a well of a first conductivity type in a substrate of a second conductivity type;
a first conductive terminal of the second conductivity type; and
an insulator between the well and the first conductive terminal.
2. The antifuse of claim 1, further comprising an ohmic contact in the well as a second conductive terminal.
3. The antifuse of claim 2 wherein:
the substrate comprises a p-type silicon substrate;
the well comprises an n-type well in the substrate;
the ohmic contact comprises an n+-type diffusion region;
the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of p-type polysilicon.
4. The antifuse of claim 2 wherein:
the substrate comprises an n-type silicon substrate;
the well comprises a p-type well in the substrate;
the ohmic contact comprises a p+-type diffusion region;
the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of n-type polysilicon.
5. An integrated circuit comprising:
a first circuit;
a second circuit; and
an antifuse coupled between the first circuit and the second circuit, the antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type;

a first conductive terminal of the second conductivity type; and
an insulator between the well and the first conductive terminal.

6. The integrated circuit of claim 5, further comprising an ohmic contact in the well as a second conductive terminal.

7. The integrated circuit of claim 6 wherein:
the substrate comprises a p-type silicon substrate;
the well comprises an n-type well in the substrate;
the ohmic contact comprises an n⁺-type diffusion region;
the insulator comprises a layer of oxide;
the first conductive terminal comprises a layer of p-type polysilicon;
the first circuit comprises a programming logic circuit; and
the second circuit comprises an external pin and a bias circuit.

8. The integrated circuit of claim 6 wherein:
the substrate comprises an n-type silicon substrate;
the well comprises a p-type well in the substrate;
the ohmic contact comprises a p⁺-type diffusion region;
the insulator comprises a layer of oxide;
the first conductive terminal comprises a layer of n-type polysilicon;
the first circuit comprises a programming logic circuit; and
the second circuit comprises an external pin and a bias circuit.

9. The integrated circuit of claim 5 wherein the integrated circuit comprises a memory device and further comprises an array of memory cells, an address decoder, a plurality of input/output paths, and an input/output control circuit.

10. An integrated circuit comprising:
 - a programming logic circuit;
 - an external pin; and
 - a plurality of antifuses, each antifuse comprising:
 - a well of a first conductivity type in a substrate of a second conductivity type, the well being coupled to the external pin;
 - a first conductive terminal of the second conductivity type coupled to the programming logic circuit; and
 - an insulator between the well and the first conductive terminal.
11. The integrated circuit of claim 10, further comprising an ohmic contact in the well coupled to the external pin.
12. The integrated circuit of claim 11 wherein:
 - the substrate comprises a p-type silicon substrate;
 - the well comprises an n-type well in the substrate;
 - the ohmic contact comprises an n⁺-type diffusion region;
 - the insulator comprises a layer of oxide; and
 - the first conductive terminal comprises a layer of p-type polysilicon.
13. The integrated circuit of claim 11 wherein:
 - the substrate comprises an n-type silicon substrate;
 - the well comprises a p-type well in the substrate;
 - the ohmic contact comprises a p⁺-type diffusion region;
 - the insulator comprises a layer of oxide; and
 - the first conductive terminal comprises a layer of n-type polysilicon.

14. The integrated circuit of claim 10 wherein the integrated circuit comprises a memory device and further comprises an array of memory cells, an address decoder, a plurality of input/output paths, and an input/output control circuit.

15. An antifuse bank comprising:

a programming logic circuit;

an external pin; and

a plurality of antifuses, each antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type, the well being coupled to the external pin;

a first conductive terminal of the second conductivity type coupled to the programming logic circuit; and

an insulator between the well and the first conductive terminal.

16. The antifuse bank of claim 15, further comprising an ohmic contact in the well coupled to the external pin.

17. The antifuse bank of claim 16 wherein:

the substrate comprises a p-type silicon substrate;

the well comprises an n-type well in the substrate;

the ohmic contact comprises an n⁺-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of p-type polysilicon.

18. The antifuse bank of claim 16 wherein:

the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;

the ohmic contact comprises a p⁺-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of n-type polysilicon.

19. A memory device comprising:
- an array of memory cells;
 - an address decoder;
 - a plurality of input/output paths;
 - an input/output control circuit; and
 - an antifuse bank comprising:
 - a programming logic circuit;
 - an external pin; and
 - a plurality of antifuses, each antifuse comprising:
 - a well of a first conductivity type in a substrate of a second conductivity type, the well being coupled to the external pin;
 - a first conductive terminal of the second conductivity type coupled to the programming logic circuit; and
 - an insulator between the well and the first conductive terminal.
20. The memory device of claim 19, further comprising an ohmic contact in the well coupled to the external pin.
21. The memory device of claim 20 wherein:
- the substrate comprises a p-type silicon substrate;
 - the well comprises an n-type well in the substrate;
 - the ohmic contact comprises an n⁺-type diffusion region;
 - the insulator comprises a layer of oxide; and
 - the first conductive terminal comprises a layer of p-type polysilicon.
22. The memory device of claim 20 wherein:
- the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;
the ohmic contact comprises a p+-type diffusion region;
the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of n-type polysilicon.

23. An integrated circuit comprising:
a circuit;
a plurality of antifuses, each antifuse comprising a first conductive terminal of a first conductivity type coupled to the circuit to receive a first programming voltage, and a well of a second conductivity type in a substrate of the first conductivity type; and
an external pin in the integrated circuit coupled to the well of each antifuse to receive a second programming voltage.
24. The integrated circuit of claim 23, further comprising an ohmic contact in the well of each antifuse coupled to the external pin.
25. The integrated circuit of claim 24 wherein:
the circuit comprises a programming logic circuit;
the substrate comprises a p-type silicon substrate;
the well comprises an n-type well in the substrate;
the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of p-type polysilicon.
26. The integrated circuit of claim 24 wherein:
the circuit comprises a programming logic circuit;
the substrate comprises an n-type silicon substrate;
the well comprises a p-type well in the substrate;

the ohmic contact comprises a p+-type diffusion region;
the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of n-type polysilicon.

27. A method comprising:

coupling a first programming voltage to a well of a first conductivity type in a substrate of a second conductivity type in an antifuse; and

coupling a second programming voltage to a conductive terminal of the second conductivity type in the antifuse to create a current path through an insulator between the conductive terminal and the well to program the antifuse.

28. The method of claim 27 wherein coupling a first programming voltage comprises coupling a first programming voltage to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the antifuse.

29. The method of claim 28 wherein:

coupling a first programming voltage comprises coupling a very high positive voltage to an n+-type diffusion region in an n-type well in a p-type substrate in an antifuse; and

coupling a second programming voltage comprises coupling a ground voltage reference to a layer of p-type polysilicon in the antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the antifuse.

30. The method of claim 28 wherein:

coupling a first programming voltage comprises coupling a very negative voltage to a p+-type diffusion region in an p-type well in an n-type substrate in an antifuse; and

coupling a second programming voltage comprises coupling a supply voltage to a layer of n-type polysilicon in the antifuse to create a current path through an insulating

layer of oxide between the layer of n-type polysilicon and the p-type well to program the antifuse.

31. A method of operating an integrated circuit comprising:
- selecting an antifuse coupled between a first circuit and a second circuit in an integrated circuit;
 - coupling a first programming voltage to a well of a first conductivity type in a substrate of a second conductivity type in the selected antifuse; and
 - coupling a second programming voltage to a conductive terminal of the second conductivity type in the selected antifuse to create a current path through an insulator between the conductive terminal and the well to program the selected antifuse.
32. The method of claim 31 wherein coupling a first programming voltage comprises coupling a first programming voltage to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the selected antifuse.
33. The method of claim 32 wherein:
- selecting an antifuse comprises selecting an antifuse from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit in the integrated circuit;
 - coupling a first programming voltage comprises coupling a very high positive voltage to the external pin that is coupled to an n⁺-type diffusion region in an n-type well in a p-type substrate in the selected antifuse; and
 - coupling a second programming voltage comprises coupling a ground voltage reference from the programming logic circuit to a layer of p-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the selected antifuse.

34. The method of claim 32 wherein:

selecting an antifuse comprises selecting an antifuse from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit in the integrated circuit;

coupling a first programming voltage comprises coupling a very negative voltage to the external pin that is coupled to a p+-type diffusion region in a p-type well in an n-type substrate in the selected antifuse; and

coupling a second programming voltage comprises coupling a supply voltage from the programming logic circuit to a layer of n-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of n-type polysilicon and the p-type well to program the selected antifuse.

35. A method of operating an integrated circuit comprising:

selecting an antifuse coupled between a circuit and an external pin in the integrated circuit;

coupling a first programming voltage to the external pin that is coupled to a well of a first conductivity type in a substrate of a second conductivity type in the selected antifuse; and

coupling a second programming voltage from the circuit to a conductive terminal of the second conductivity type in the selected antifuse to create a current path through an insulator between the conductive terminal and the well to program the selected antifuse.

36. The method of claim 35 wherein coupling a first programming voltage comprises coupling a first programming voltage to the external pin that is coupled to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the selected antifuse.

1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378</
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coupling a second programming voltage comprises coupling a ground voltage reference from the programming logic circuit to a layer of p-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the selected antifuse.

coupling a first programming voltage comprises coupling a very negative voltage to the external pin that is coupled to a p+-type diffusion region in a p-type well in an n-type substrate in the selected antifuse; and

39. A method comprising:

programming an antifuse in the system to couple two or more of the selected s together, comprising:

coupling a first programming voltage to a well of a first conductivity type in a substrate of a second conductivity type in the antifuse; and

coupling a second programming voltage to a conductive terminal of the second conductivity type in the antifuse to create a current path through an insulator between the conductive terminal and the well to program the antifuse.

40. The method of claim 39 wherein coupling a first programming voltage comprises coupling a first programming voltage to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the antifuse.

41. The method of claim 40 wherein:

coupling a first programming voltage comprises coupling a very high positive voltage to an n⁺-type diffusion region in an n-type well in a p-type substrate in the antifuse; and

coupling a second programming voltage comprises coupling a ground voltage reference to a layer of p-type polysilicon in the antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the antifuse.

42. The method of claim 40 wherein:

coupling a first programming voltage comprises coupling a very negative voltage to a p⁺-type diffusion region in an p-type well in an n-type substrate in the antifuse; and

coupling a second programming voltage comprises coupling a supply voltage to a layer of n-type polysilicon in the antifuse to create a current path through an insulating layer of oxide between the layer of n-type polysilicon and the p-type well to program the antifuse.

43. A method of forming an antifuse comprising:
forming a well of a first conductivity type in a substrate of a second conductivity type;
forming an insulator over the well; and
forming a first conductive terminal of the second conductivity type over the insulator.

44. The method of claim 43, further comprising forming an ohmic contact in the well as a second conductive terminal.

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45. The method of claim 43 wherein:
forming a well comprises forming an n-type well in a p-type silicon substrate and further comprises:
forming an n+-type diffusion region in the well;
forming an n+-type drain diffusion region in the well;
forming an n+-type source diffusion region in the well;
forming an insulator comprises forming a layer of oxide over the well between the drain diffusion region and the source diffusion region; and
forming a first conductive terminal comprises forming a p-type polysilicon gate electrode over the layer of oxide.

46. The method of claim 43 wherein:
forming a well comprises forming a p-type well in an n-type silicon substrate and further comprises:
forming a p+-type diffusion region in the well;
forming a p+-type drain diffusion region in the well;
forming a p+-type source diffusion region in the well;

forming an insulator comprises forming a layer of oxide over the well between the drain diffusion region and the source diffusion region; and

forming a first conductive terminal comprises forming an n-type polysilicon gate electrode over the layer of oxide.

47. An antifuse comprising:
a body isolated by an isolation insulator;
a conductive terminal; and
a gate insulator between the body and the first conductive terminal.
48. The antifuse of claim 47, further comprising:
an ohmic contact in the body; and
wherein the body comprises silicon isolated by the isolation insulator.
49. The antifuse of claim 48 wherein:
the body comprises n-type silicon;
the ohmic contact comprises an n+-type diffusion region in the body;
the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;
the gate insulator comprises a layer of oxide; and
the conductive terminal comprises a layer of n+-type polysilicon.
50. The antifuse of claim 48 wherein:
the body comprises p-type silicon;
the ohmic contact comprises a p+-type diffusion region in the body;
the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and
the conductive terminal comprises a layer of p+-type polysilicon.

51. The antifuse of claim 48 wherein:
the body comprises n-type silicon;
the ohmic contact comprises an n+-type diffusion region in the body;
the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and
the conductive terminal comprises a layer of p+-type polysilicon.

52. The antifuse of claim 48 wherein:
the body comprises p-type silicon;
the ohmic contact comprises a p+-type diffusion region in the body;
the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and
the conductive terminal comprises a layer of n+-type polysilicon.